REMARKS

Applicants respectfully request further examination and reconsideration in view of the above amendments. Claims 1-3, 5-9, 12, 13 and 18-20 remain pending in the case. Claims 1-3, 5-9, 12, 13 and 18-20 are rejected. Claims 1, 8, 12, 13, 18 and 19 are amended herein. No new matter has been added.

35 U.S.C. §103(a)

Claims 1-3, 5-9, 12, 13 and 18-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over United States Patent 5,437,017 by Moore et al., hereinafter referred to as the "Moore" reference, in view of "IBM Technical Disclosure Bulletin, May 1994, Vol. 37, Issue 5, pages 249-250 hereinafter referred to as the "IBMTDB 37" reference. Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 1-3, 5-9, 12, 13 and 18-20 are not unpatentable over Moore in view of IBMTDB 37 for the following rationale.

Applicants respectfully direct the Examiner to independent Claim 1 that recites that an embodiment of the present invention is directed to (emphasis added):

> A system for maintaining translation consistency in a computer which includes a host processor designed to execute instructions of a host instruction set and software for translating instructions from a target instruction set to instructions of the host instruction set comprising:
>
> hardware means for indicating whether a memory address to be written stores a target instruction which has been translated

to at least one host instruction, the host instruction for execution by the host processor; and

software means responding to an indication that a memory address to be written stores a target instruction which has been translated to at least one host instruction for assuring that host instructions translated from the target instructions stored at the memory address will not be utilized once the memory address has been written.

Claims 7, 12 and 18 provide similar limitations. Claims 2, 3, 5 and 6 that depend from independent Claim 1, Claims 8 and 9 that depend from independent Claim 7, Claim 13 that depends from independent Claim 12, and Claims 19 and 20 that depend from independent Claim 18 provide further recitations of the features of the present invention.

Applicants respectfully assert that the combination of Moore and IBMTDB 37 does not teach, describe or suggest the embodiments of the present invention recited in Claim 1. For instance, Moore and the present invention are very different. Applicants understand Moore to teach a method and system for maintaining translation lookaside buffer (TLB) coherency in a multiprocessor data processing system. In particular, Moore teaches a multiprocessor system including multiple TLBs, each associated with a different processor, for maintaining coherency between all TLBs of the multiprocessor system (Abstract; col. 2, line 66 through col. 3, line 3; col. 4, lines 25-30).

Applicants respectfully assert that Moore does not teach, describe or suggest a system for maintaining translation consistency in a computer which

includes a host processor including "hardware means for indicating whether a memory address to be written stores a target instruction which has been translated to at least one host instruction, the host instruction for execution by the host processor," as claimed (emphasis added). With reference to Figure 1 of Moore, a multi-processor data processing system 6 includes multiple processors 10, each processor 10 including a TLB 40. The TLB is used for translating effective or virtual addresses into real addresses within system memory 18.

In particular, because each processor 10 accesses system memory 18, coherency between all TLBs 40 must be maintained (col. 4, lines 19-30). As described in Moore, each TLB 40 must include the real address for each instruction executable by each processor 10 (col. 6, line 65 through col. 7, line 2). In other words, each TLB 40 will include instructions that are not associated with its corresponding processor 10, but rather for execution by another processor 10.

Applicants understand that the TLBs as taught in Moore are used for maintaining address translations of a multi-processor system. Moore teaches that a translation lookaside buffer invalidate (TLBI) instruction is executed by one processor of the multi-processor system for broadcasting the TLBI instruction to other processors of the multi-processor system (col. 3, lines 3-21; col. 8, lines 39-44). In particular, Applicants respectfully assert that a TLBI

instruction is initiated in response to the modification of the translation relationship stored within one TLB of the multiple TLBs (col. 7, lines 3-18). Moreover, Moore teaches that each processor of the multi-processor system must execute the TLBI instruction in order to synchronize the TLBs (col. 8, lines 11-18).

In contrast, the present invention provides a system for maintaining translation consistency in a computer which includes a host processor including "hardware means for indicating whether a memory address to be written stores a target instruction which has been translated to at least one host instruction, the host instruction for execution by the host processor," as claimed (emphasis added). As described in the specification, target instructions are translated into host instructions that are stored in a memory data structure (e.g., translation buffer) (page 24, line 24 through page 25, line 1). A translated host instruction may be stored in the memory. In particular, each translated host instruction is for execution by the host processor. In other words, the memory data structure does not include instructions for execution by other processors.

Furthermore, the claimed invention is for "maintaining translation consistency in a computer system which includes a host processor." The translation is performed by code morphing software of a single processor (page 22, line 17 through page 24, line 14). By holding translated instructions,

the translated instructions may be efficiently recalled without rerunning an extensive translation process each time the target instruction or group of instructions is executed (page 25, lines 1-12). In particular, the present invention is directed towards maintaining consistency between translated instructions.

Applicants respectfully assert that Moore does not teach, describe or suggest a system for maintaining translation consistency in a computer which includes a host processor including "hardware means for indicating whether a memory address to be written stores a target instruction which has been translated to at least one host instruction, the host instruction for execution by the host processor," as claimed. Rather, by teaching a multi-processor system in which instructions for all processors are stored on each TLB, Moore teaches away from the claimed invention. Moreover, the coherence of each TLB as described in Moore is not equivalent to the consistency between translated instructions of the present invention. The coherence of Moore is directed toward assuring that each TLB, and thus each processor, includes the same information. In contrast, the consistency between translated instructions of the present invention is related to consistency between the target instruction set and the host instruction set of a single processor.

Moreover, the combination of Moore and IBMTDB 37 fails to teach or suggest the claimed embodiments because IBMTDB 37 does not overcome

the shortcomings of Moore. IBMTDB 37, either alone or in combination with Moore, does not show or suggest the invention as claimed. Applicants understand IBMTDB 37 to teach the use of the SYNC instruction to synchronize completion of TLB invalidate across processors in a multi-processor system.

Applicants respectfully assert that IBMTDB 37 does not teach, describe or suggest a system for maintaining translation consistency in a computer which includes a host processor including "hardware means for indicating whether a memory address to be written stores a target instruction which has been translated to at least one host instruction, the host instruction for execution by the host processor," as claimed (emphasis added). As described above with reference to Moore, Applicants understand the TLB of IBMTDB 37 to store translated addresses for use in a multi-processor system. In particular, IBMTDB 37 does not teach, describe or suggest translating instructions of a target instruction set into a host instruction set, wherein the host instruction set is for execution by the host processor.

In contrast, as described in the current specification and claimed, the present invention provides that target instructions are translated into host instructions that are stored in a memory data structure. In particular, the host instructions are for execution by the host processor, as there is only one processor. By teaching a multi-processor system in which instructions for all

processors are stored on each TLB, IBMTDB 37 teaches away from the claimed invention.

Applicants respectfully assert that nowhere does the combination of Moore and IBMTDB 37 teach, disclose or suggest the present invention as recited in independent Claims 1, 7, 12 and 18, and that Claims 1, 7, 12 and 18 are thus in condition for allowance. Therefore, Applicants respectfully submit that the combination of Moore and IBMTDB 37 also does not teach or suggest the additional claimed features of the present invention as recited in Claims 2, 3, 5 and 6 that depend from independent Claim 1, Claims 8 and 9 that depend from independent Claim 7, Claim 13 that depends from independent Claim 12, and Claims 19 and 20 that depend from independent Claim 18. Applicants respectfully submit that Claims 2, 3, 5, 6, 8, 9, 13, 19 and 20 overcome the rejection under 35 U.S.C. § 103(a) as these claims are dependent on an allowable base claim.

CONCLUSION

In light of the above remarks, Applicants respectfully request reconsideration of the rejected claims. Based on the arguments presented above, Applicants respectfully assert that Claims 1-3, 5-9, 12, 13 and 18-20 overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these Claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,
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